

FIG.1(a)

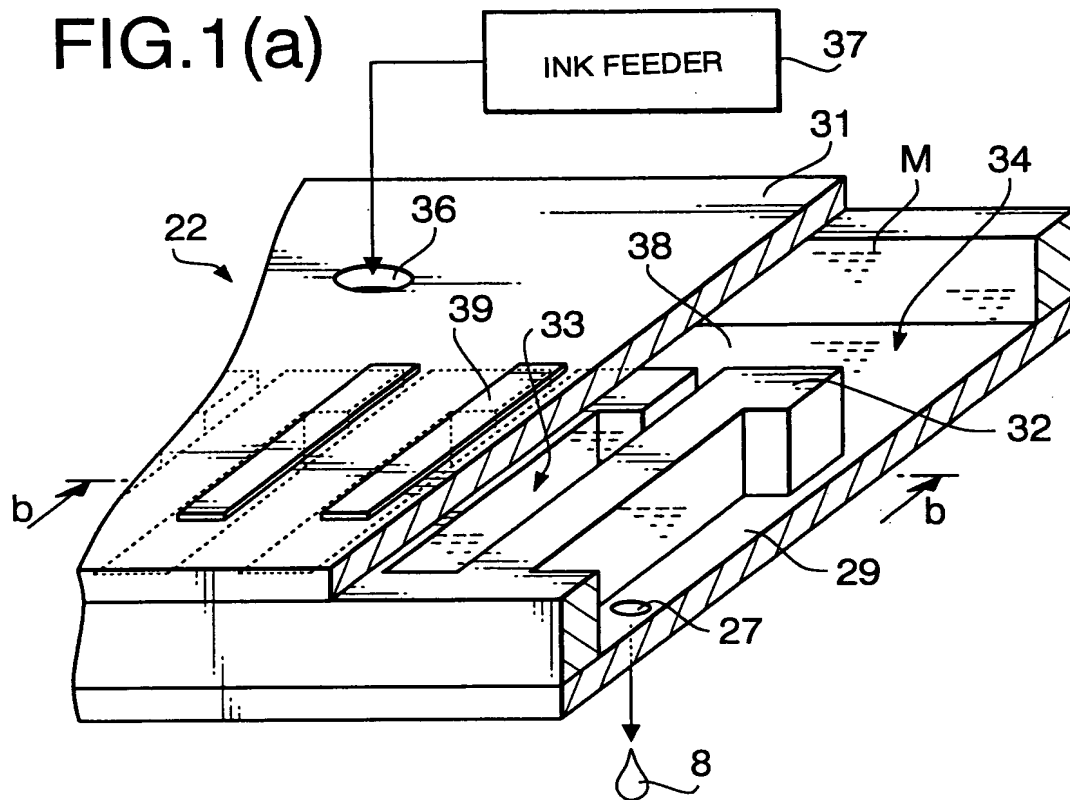


FIG.1(b)

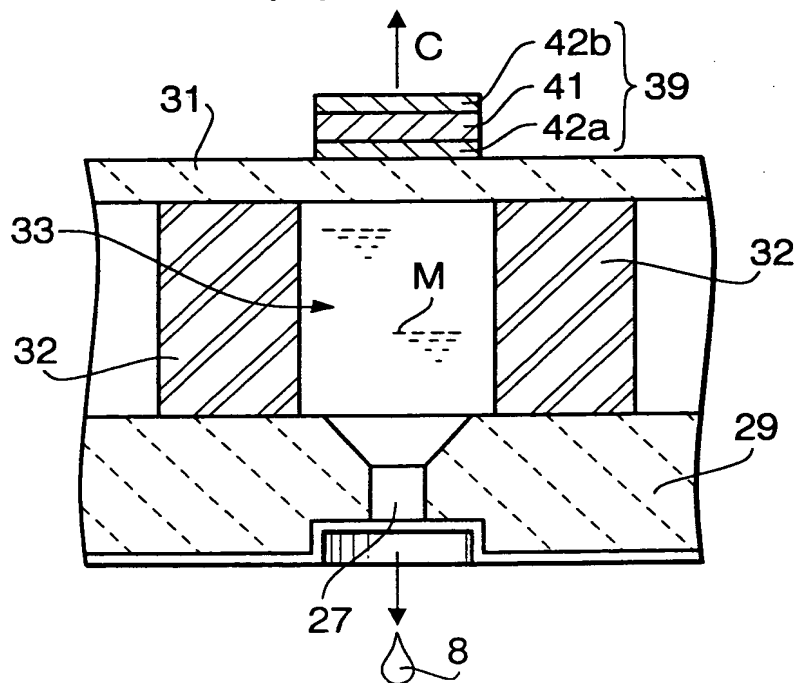


FIG.2(a)

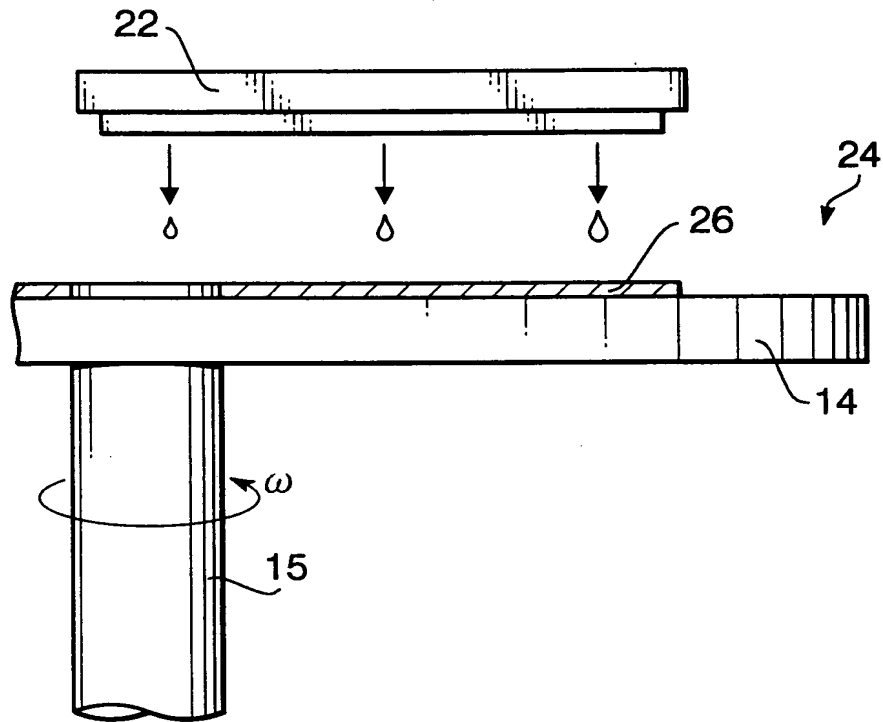


FIG.2(b)

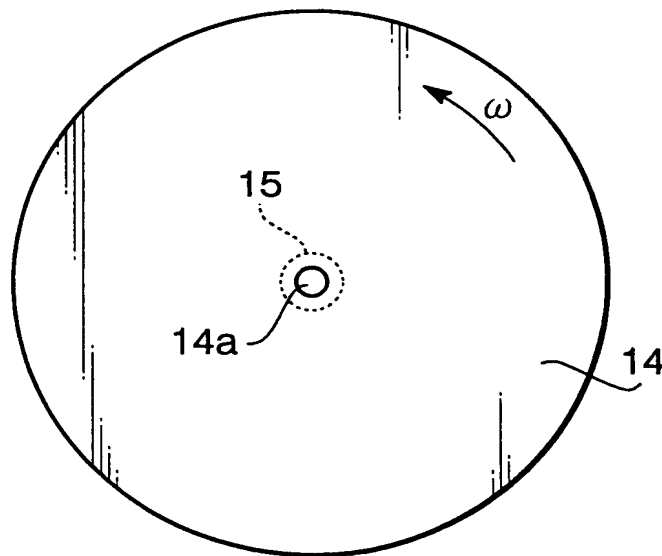


FIG. 3

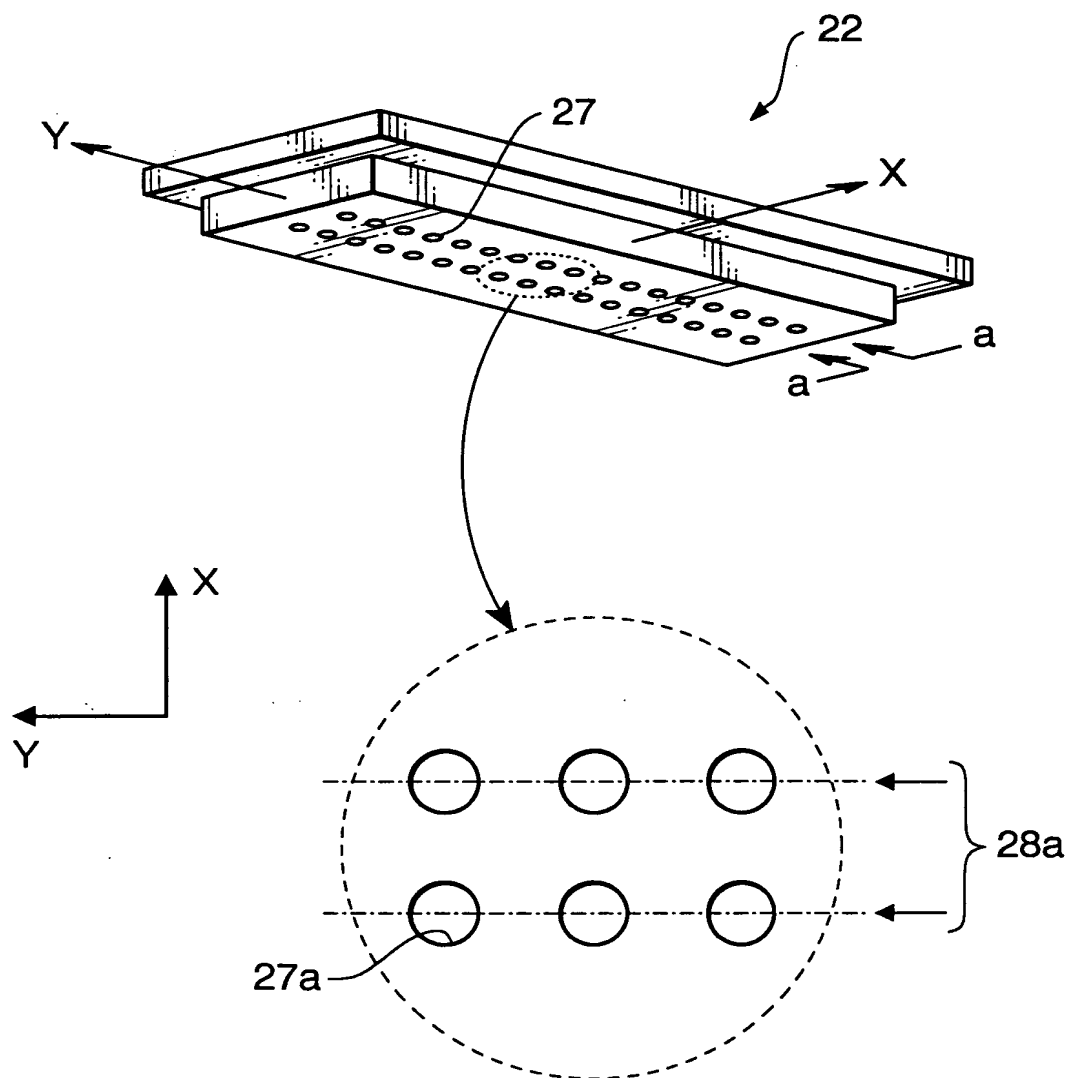


FIG. 4

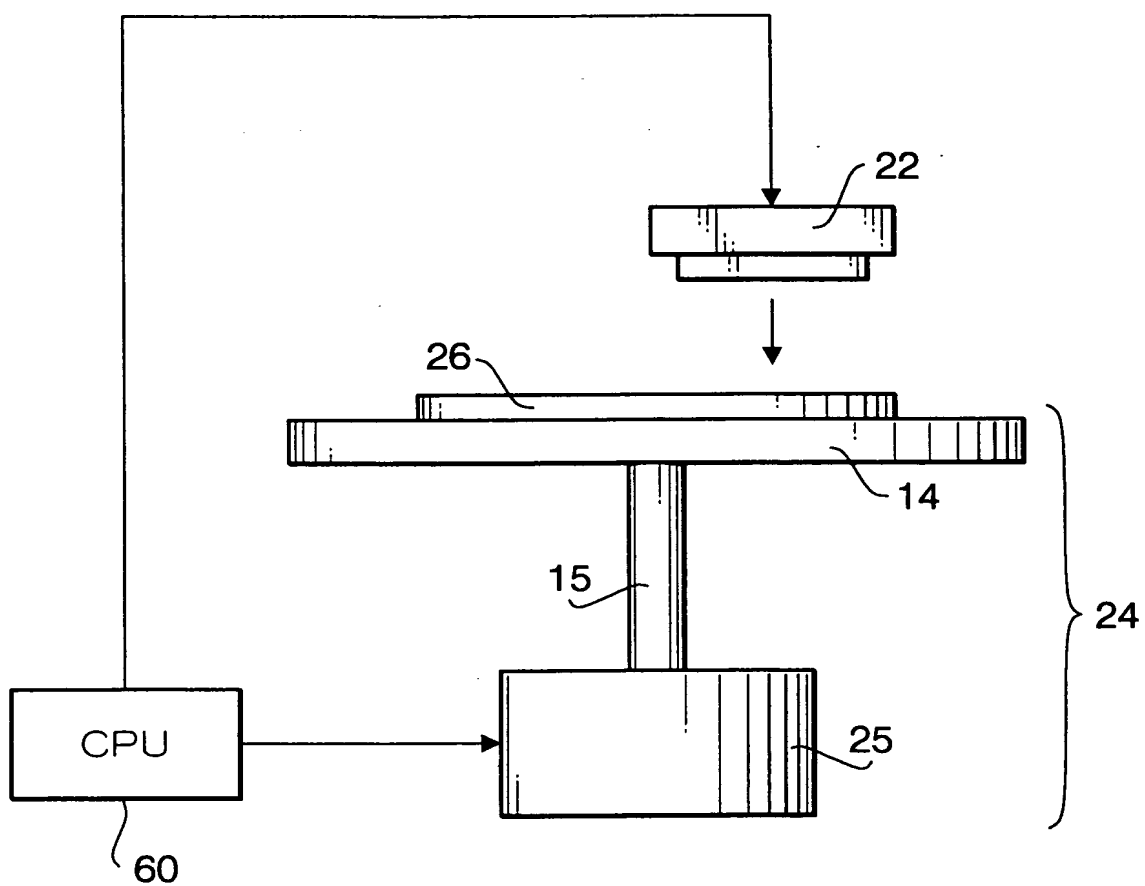


FIG.5(a)

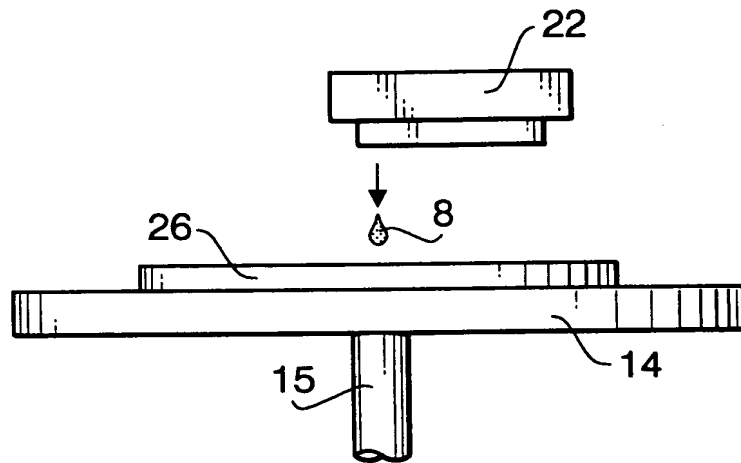


FIG.5(b)

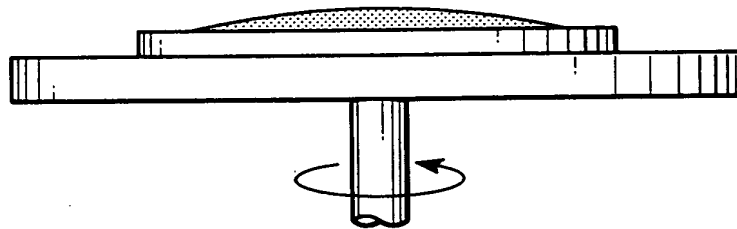


FIG.5(c)

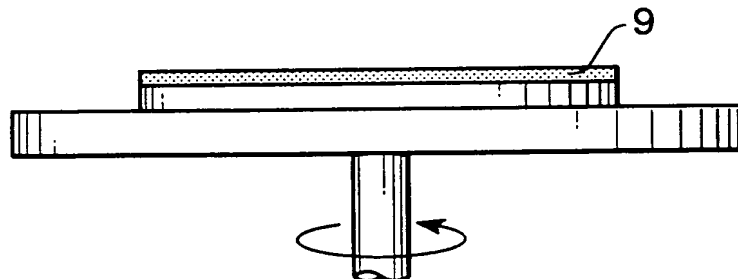
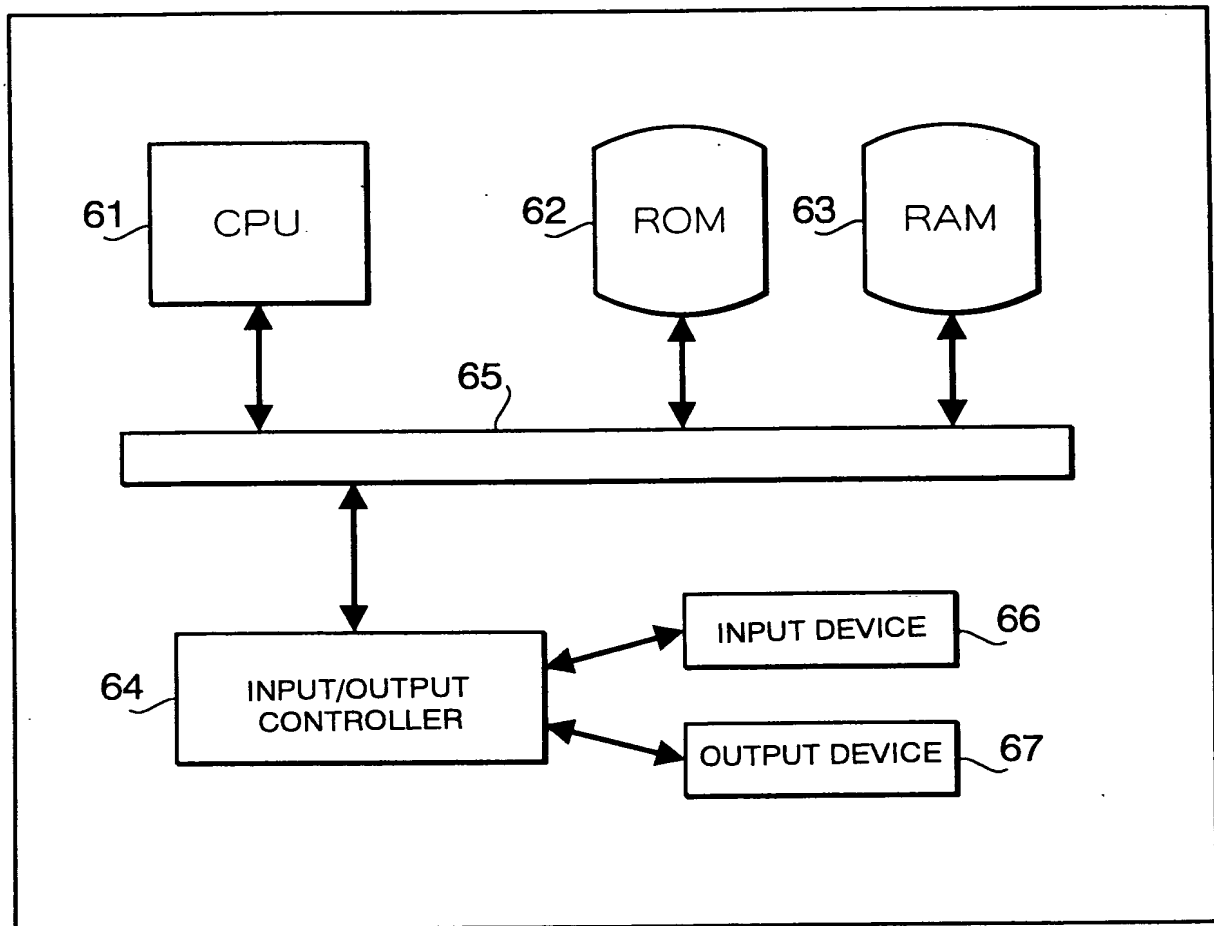


FIG. 6



HOST COMPUTER 60

FIG.7(a)

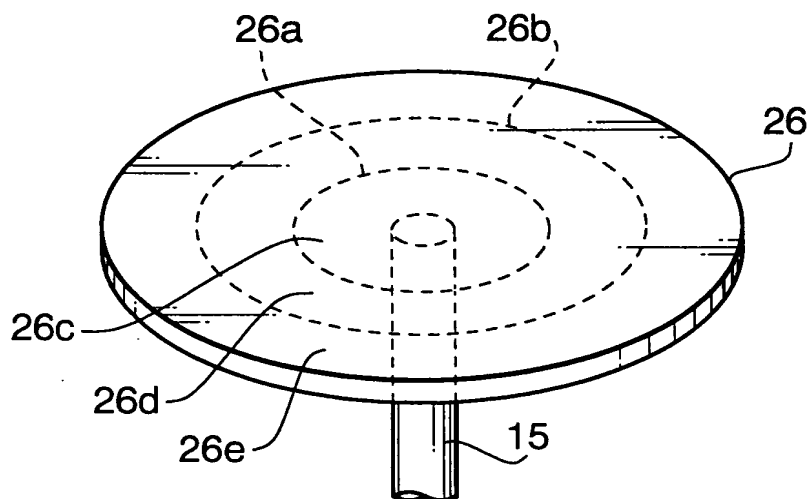


FIG.7(b)

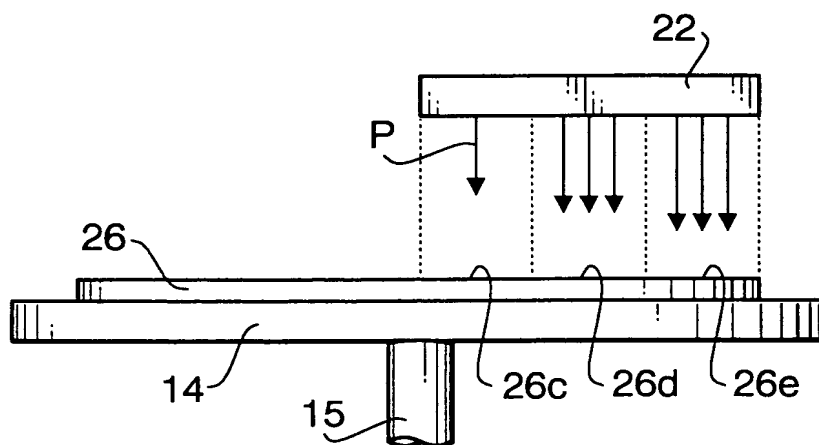


FIG.8(a)

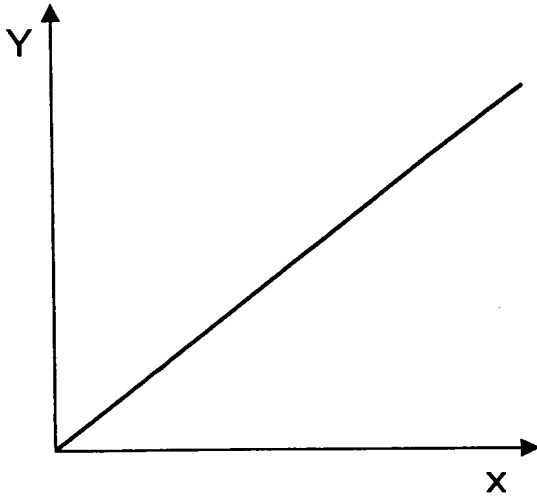


FIG.8(b)

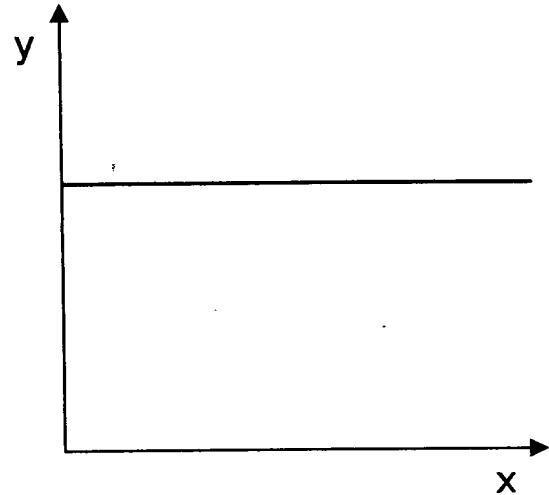


FIG.9(a)

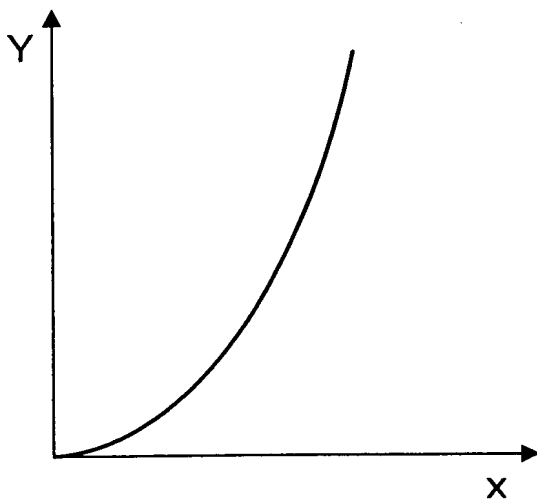


FIG.9(b)

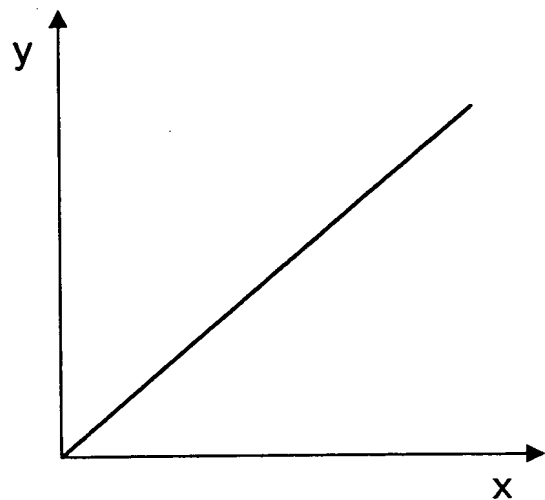


FIG.10(a)

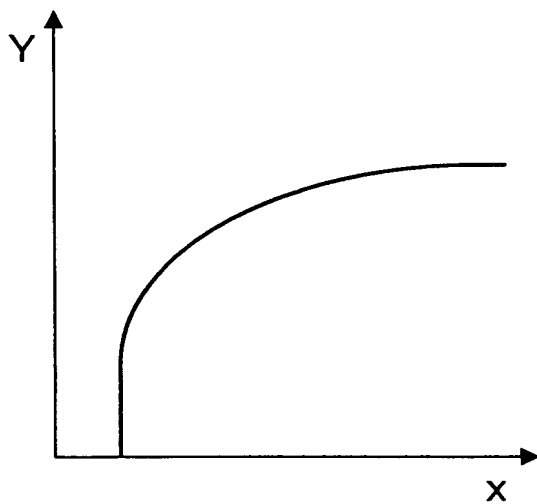


FIG.10(b)

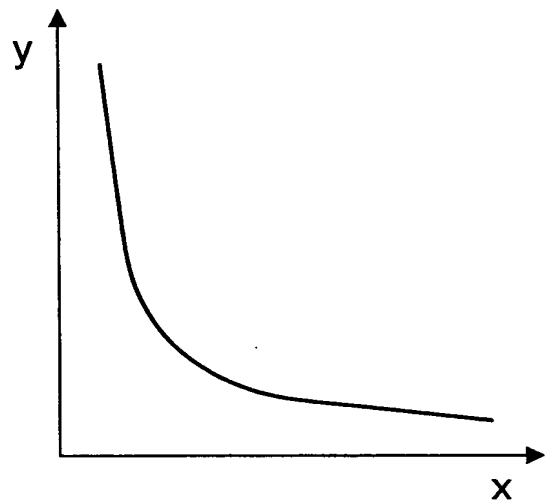


FIG.11(a)

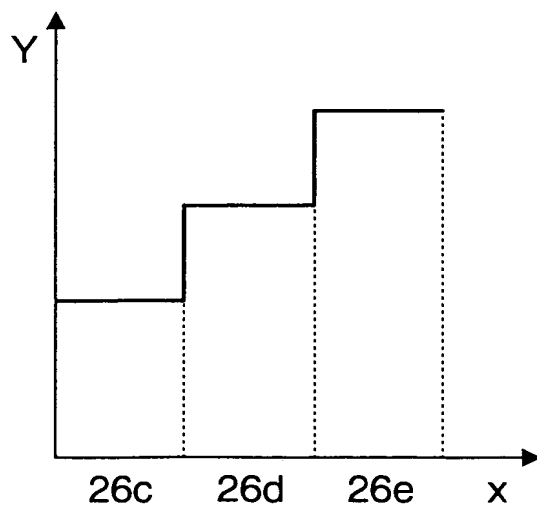


FIG.11(b)

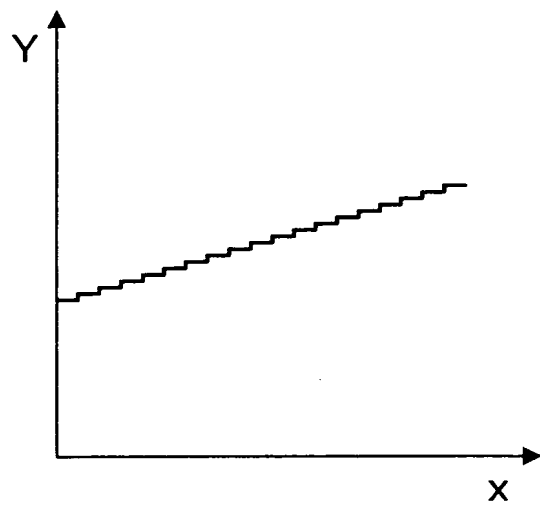


FIG.12

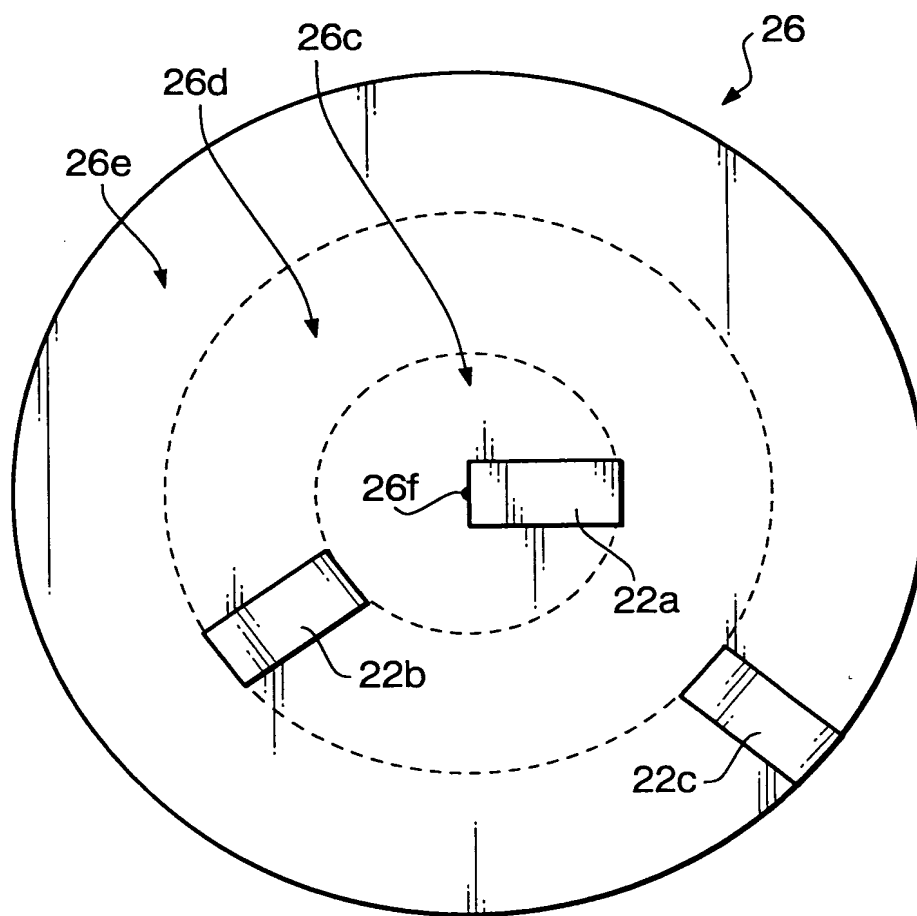


FIG.13

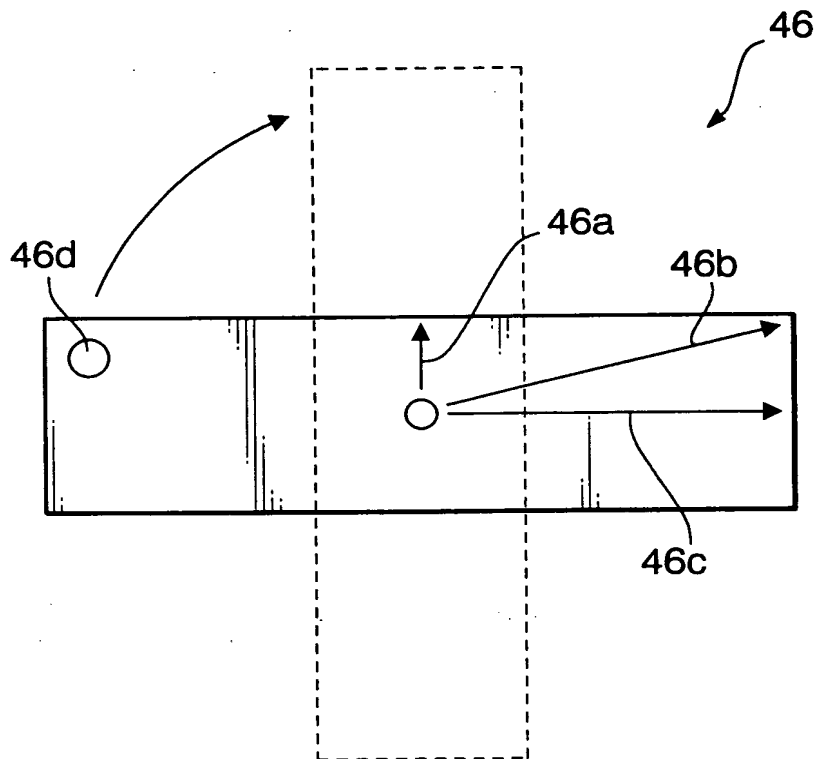


FIG.14(a)

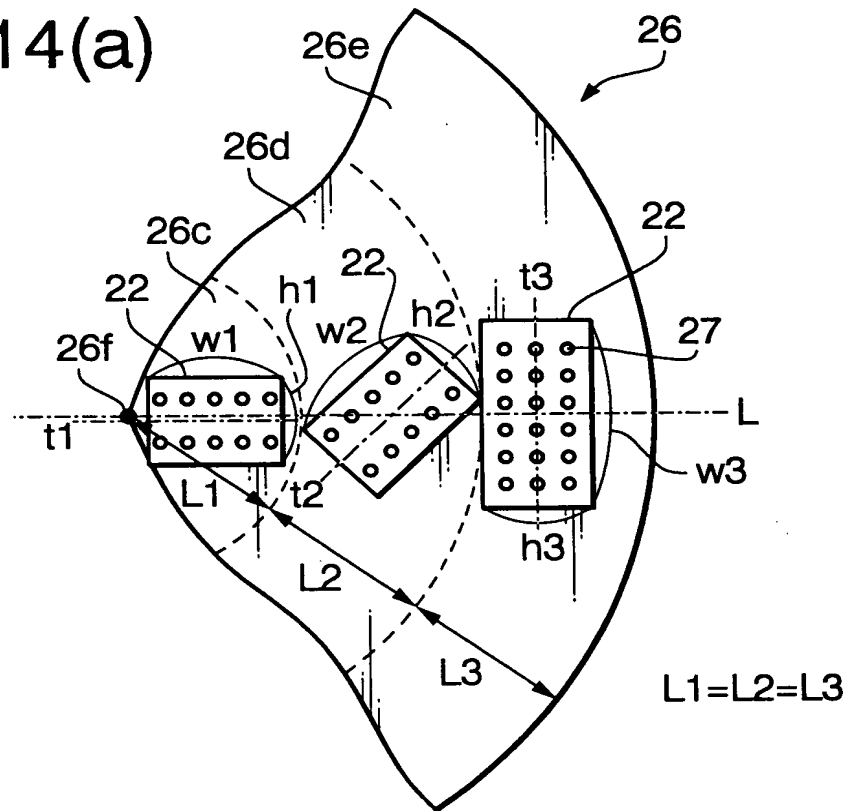


FIG.14(b)

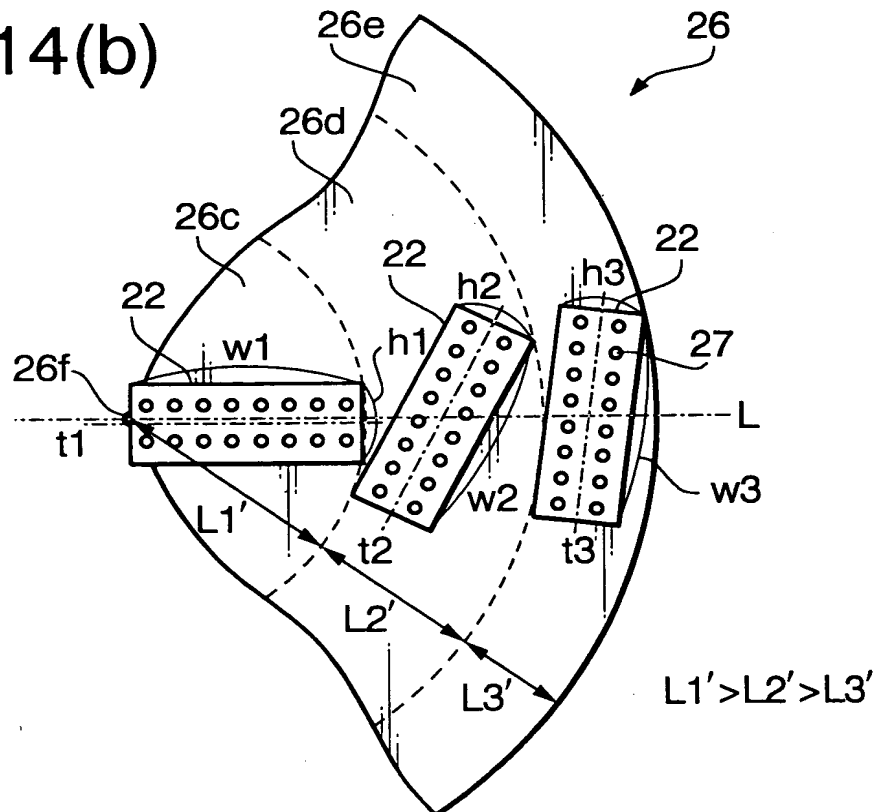


FIG.15

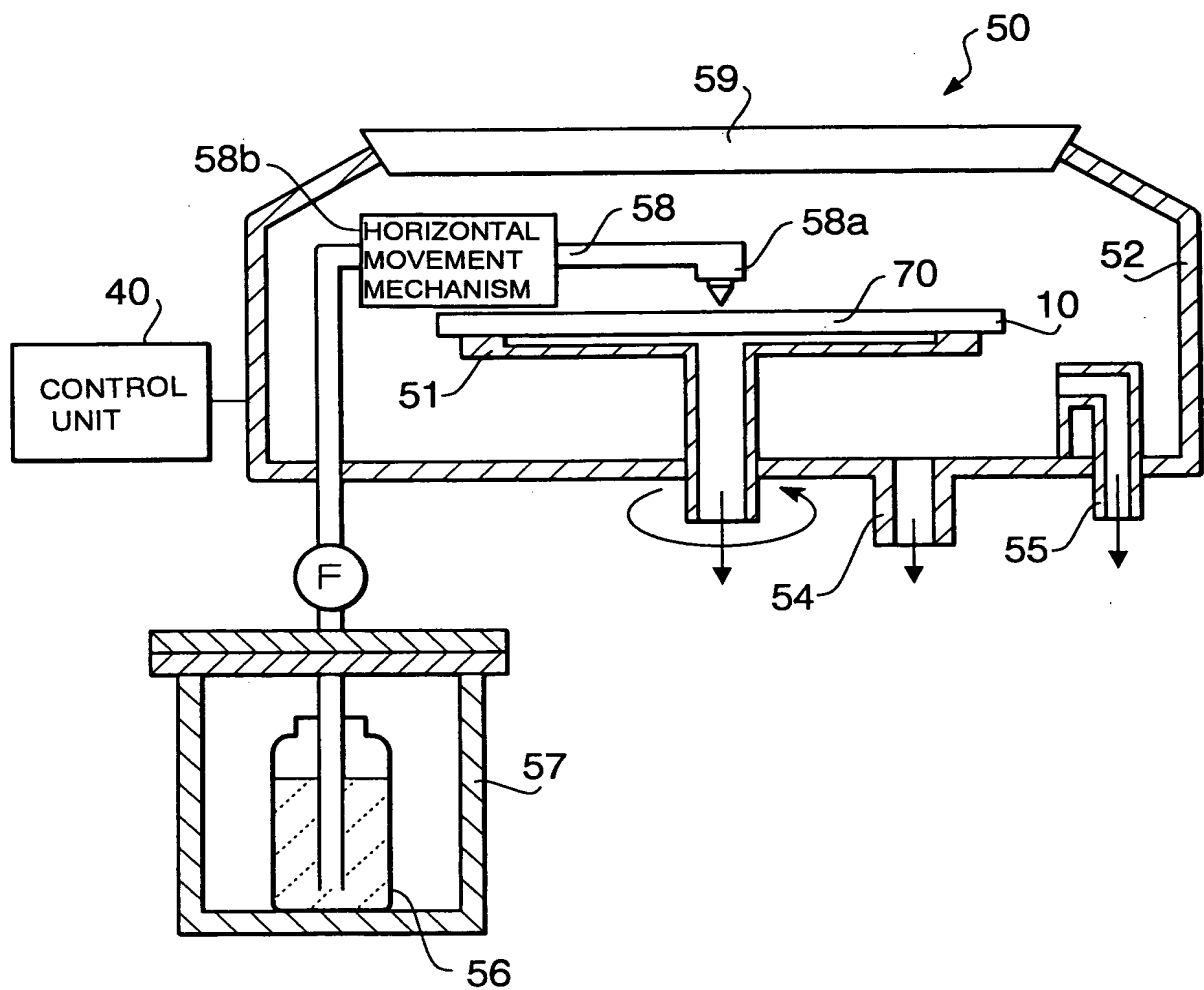
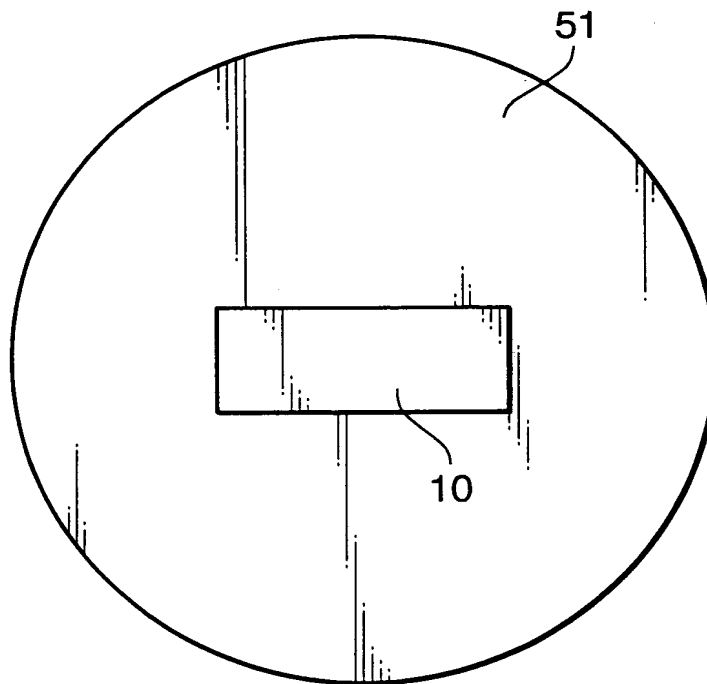
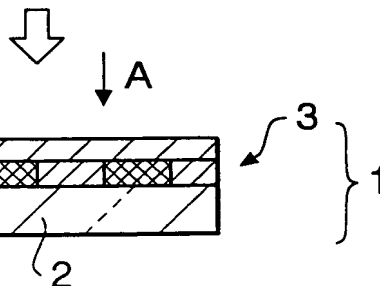
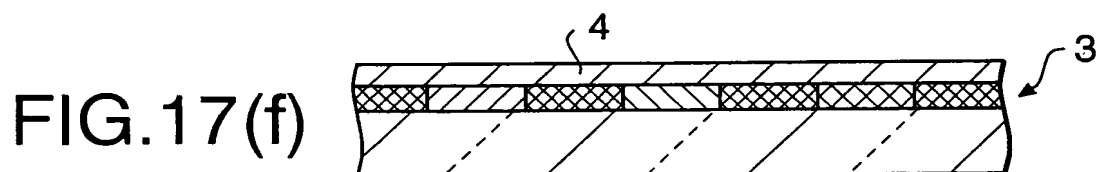
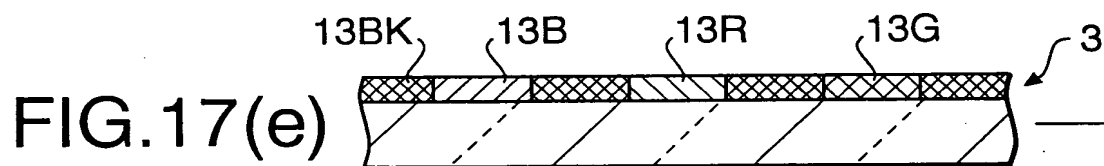
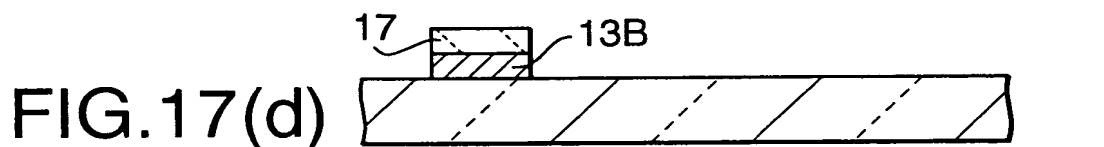
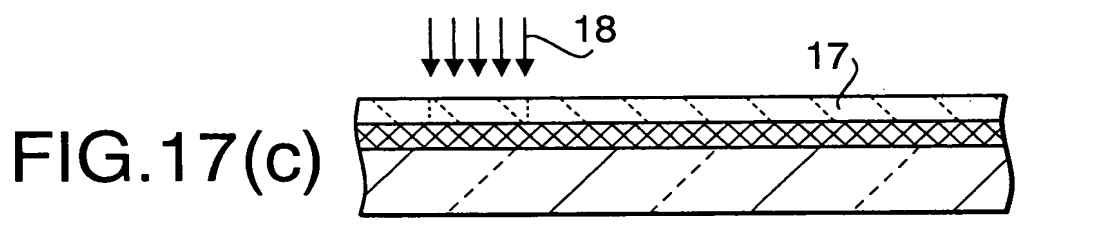
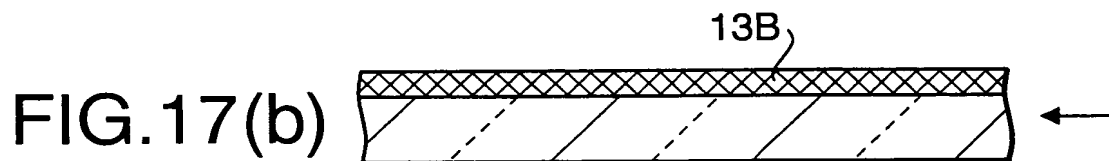
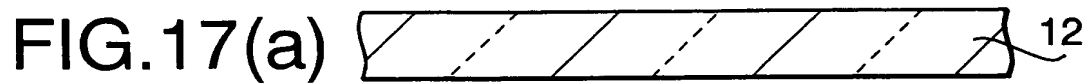


FIG.16





REPEAT 4 TIMES

FIG.18(a)

STRIPE

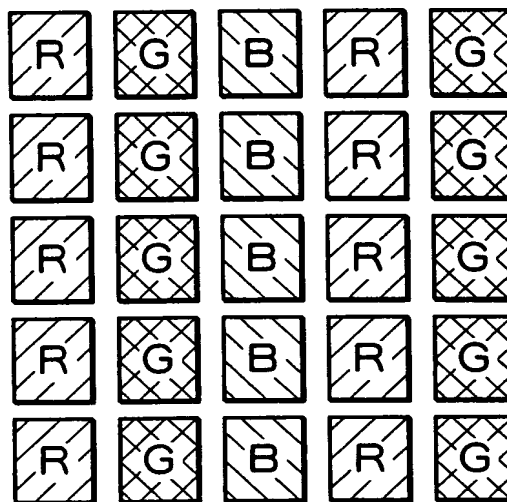


FIG.18(b)

MOSAIC

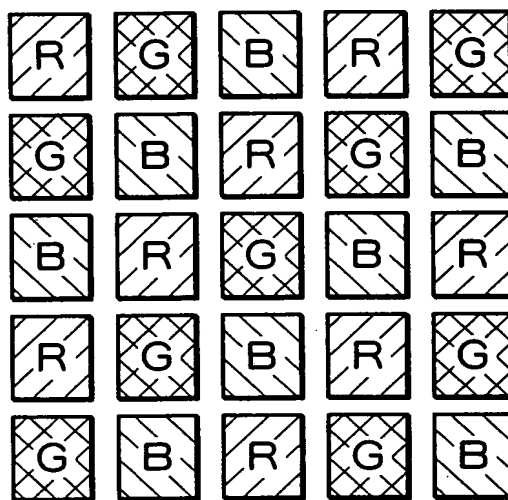


FIG.18(c)

DELTA

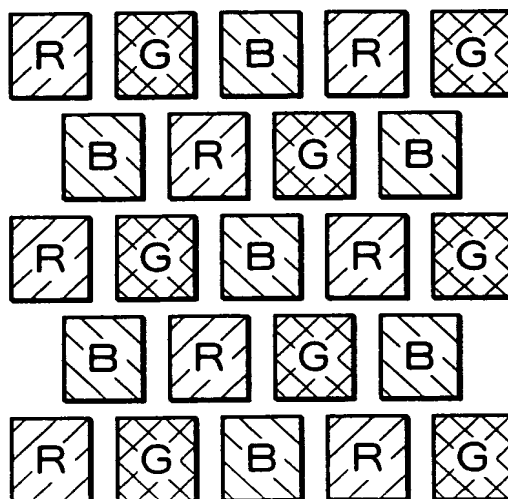


FIG.19

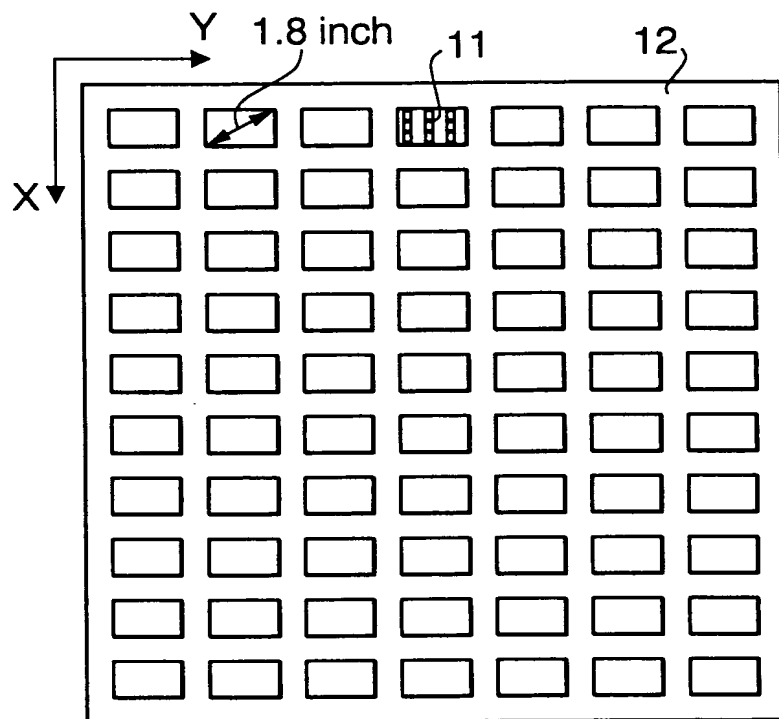


FIG.20

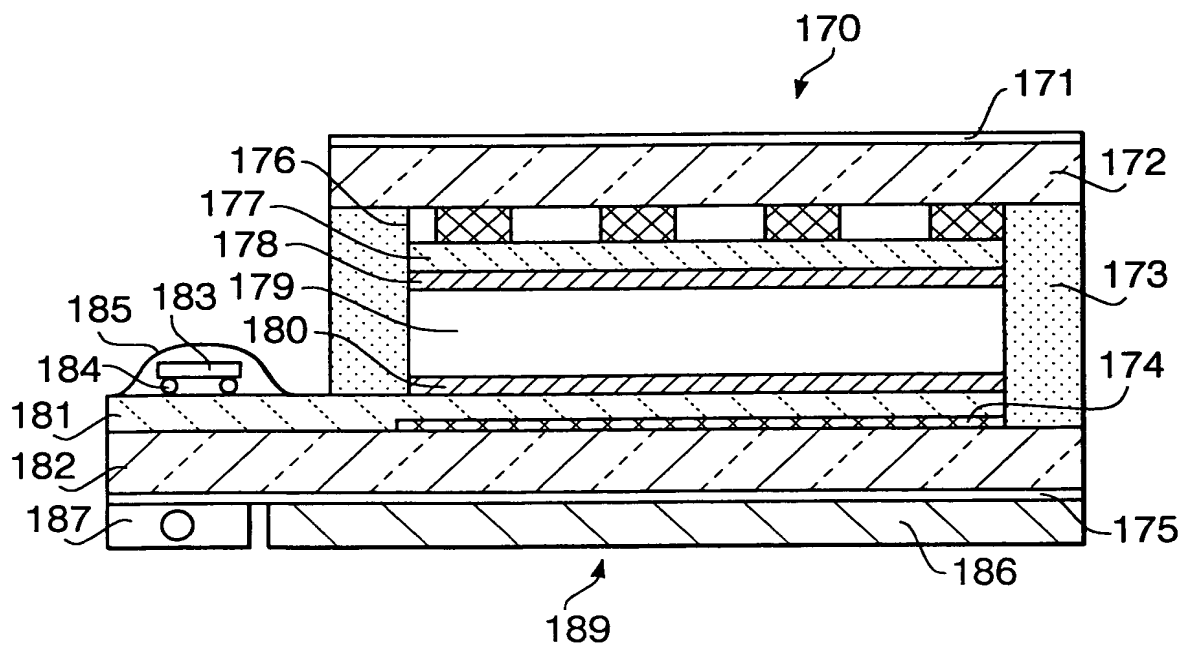
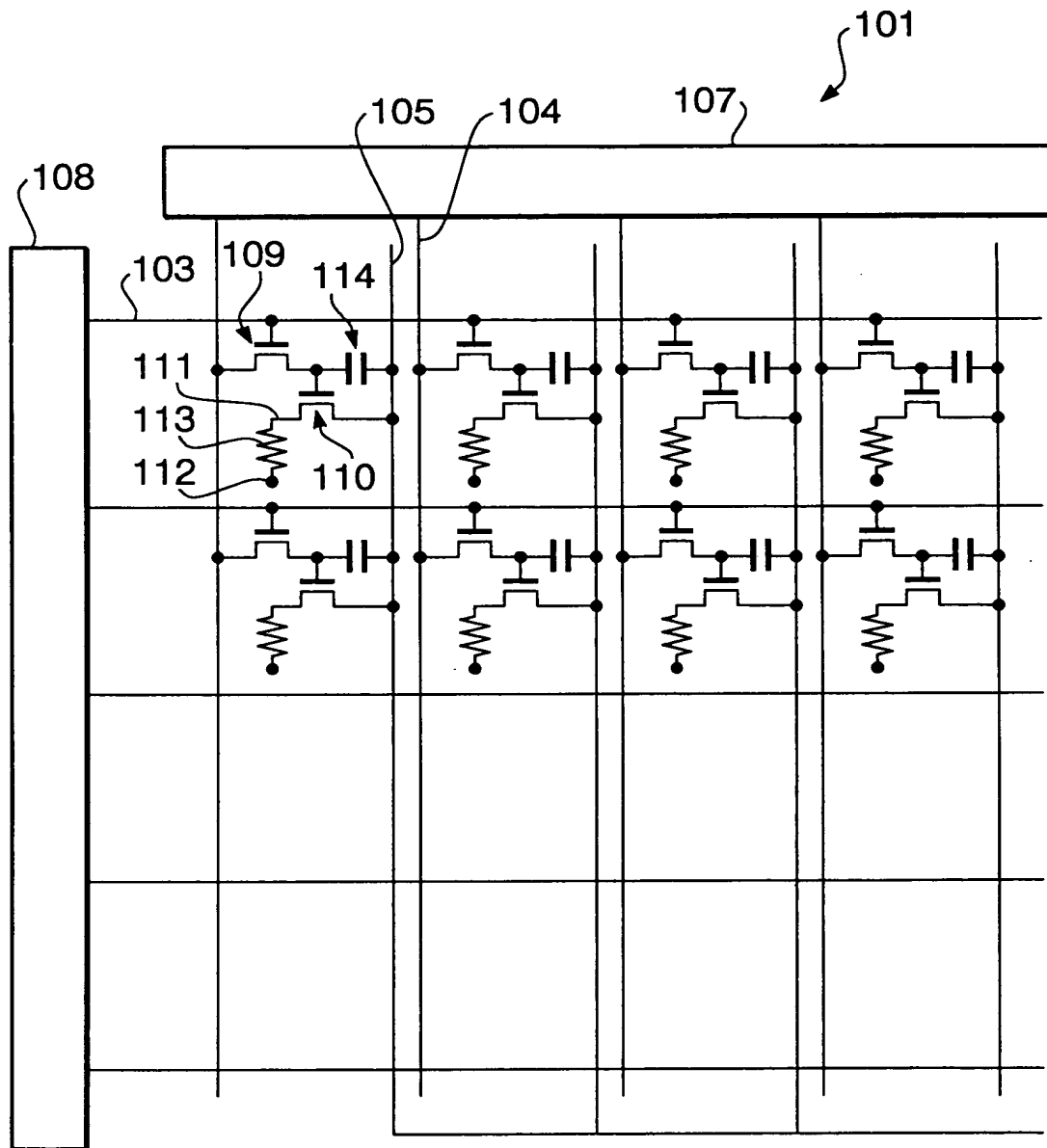


FIG.21



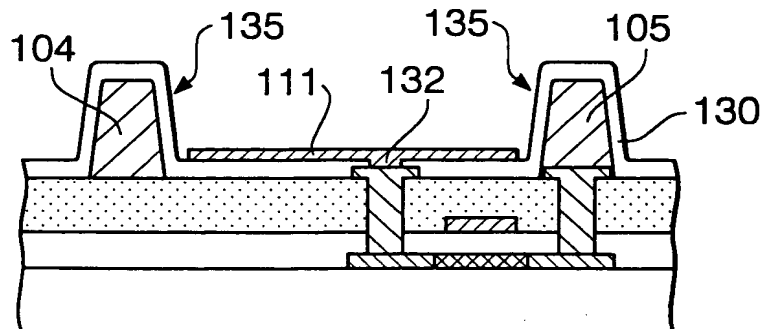
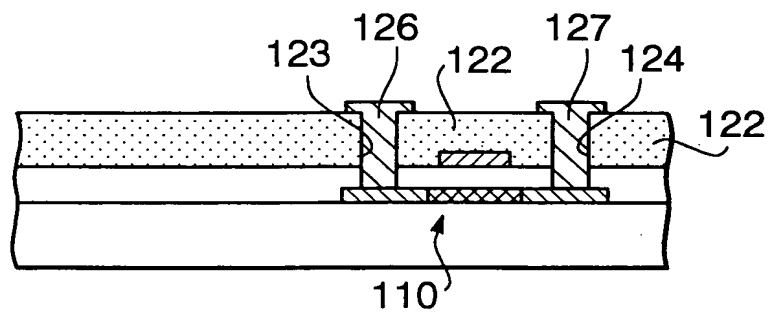
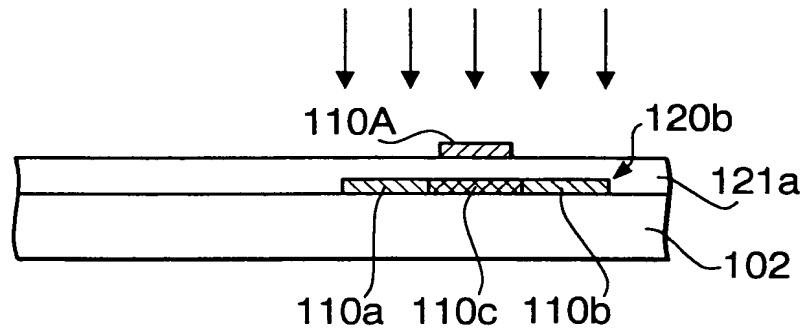
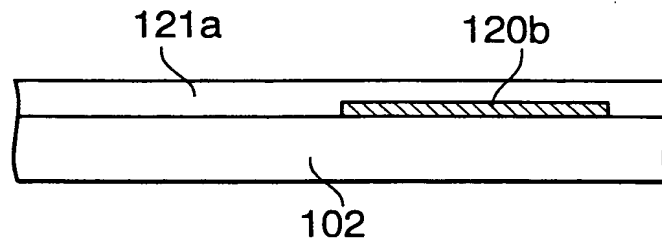
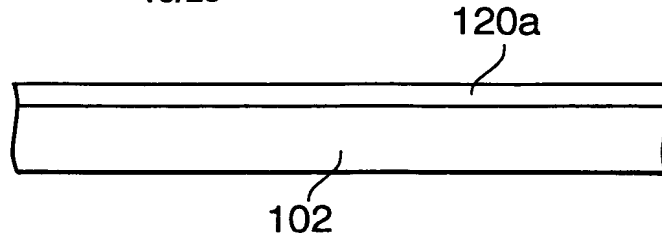


FIG.23(a)

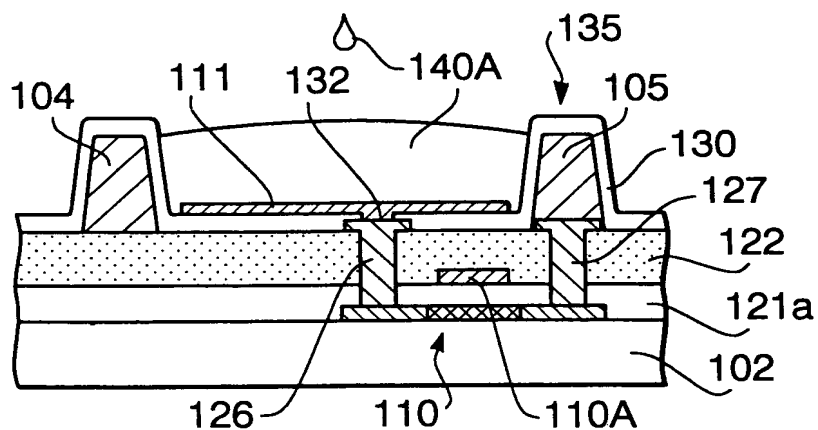


FIG.23(b)

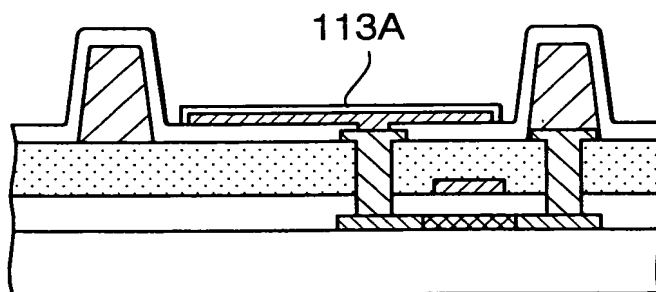
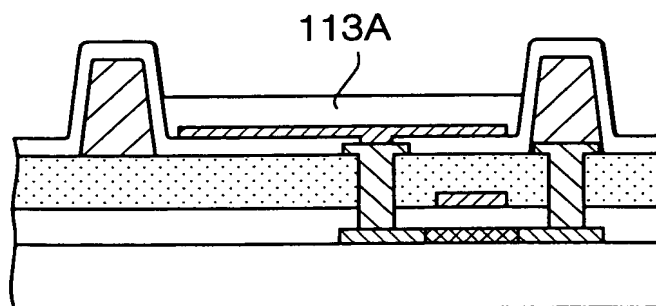


FIG.23(c)



113B

This cross-sectional view shows a gate structure 113B. It features a central gate stack with a core layer and a gate dielectric layer, flanked by side spacers. The gate stack is positioned on a substrate with a patterned layer underneath. The side spacers are shown with a cross-hatched pattern, and the substrate has a dotted pattern.

A cross-sectional view of a semiconductor device. A gate stack, labeled 113, is positioned over a channel region. The gate stack consists of a gate dielectric layer 113B and a gate conductive layer 113A. The channel region is defined by source/drain regions on either side, which are doped with impurities (indicated by diagonal hatching). The substrate is a silicon wafer (indicated by a dotted pattern).

A cross-sectional view of a semiconductor device. It shows a substrate with a central region containing a horizontal layer. Above this, there are two trapezoidal structures on either side of a central gap. A layer with a cross-hatched pattern, labeled 112, covers the top of the trapezoidal structures and the central gap. Below the central gap, there is a small rectangular feature. The entire structure is supported by a base layer with a dotted pattern.

FIG.25

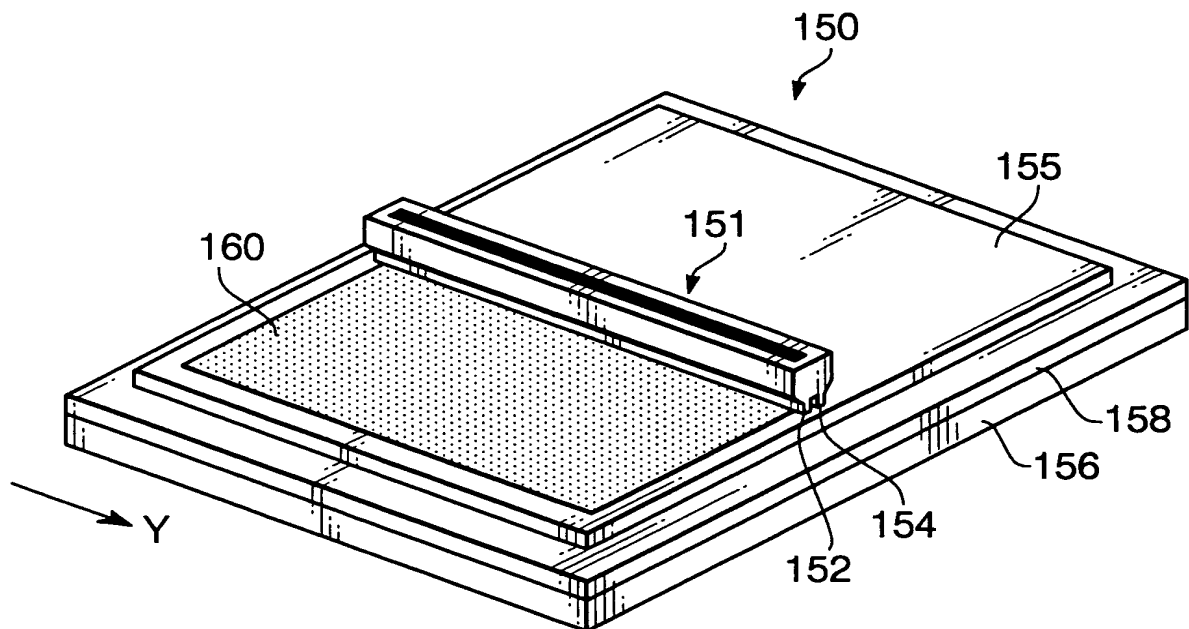


FIG.26  
(PRIOR ART)

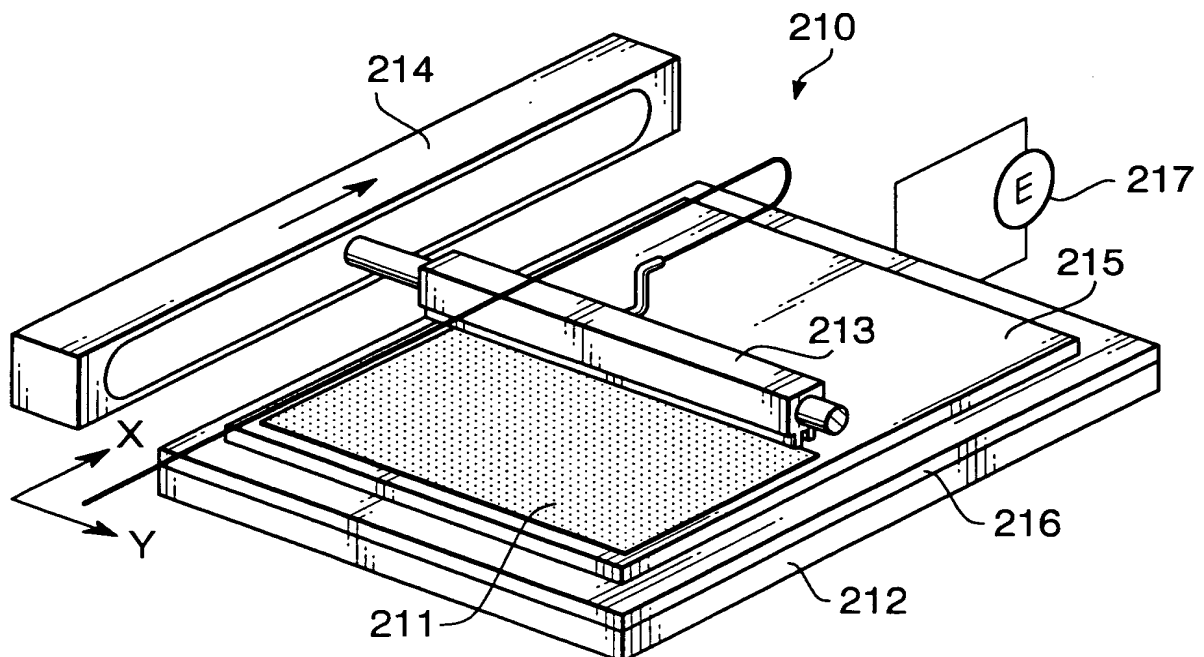


FIG.27

(PRIOR ART)

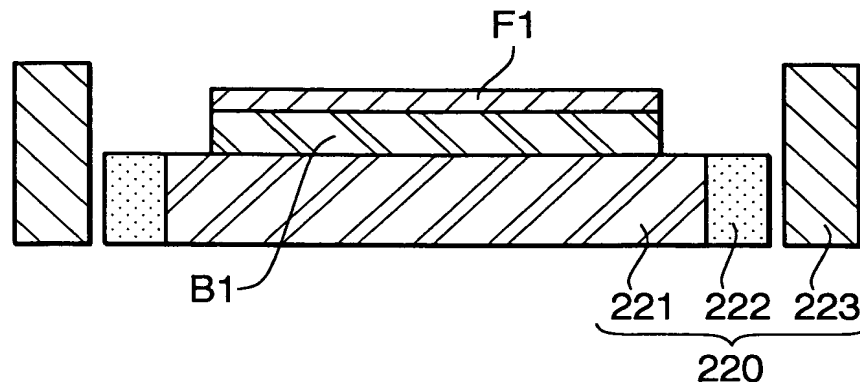


FIG.28

(PRIOR ART)

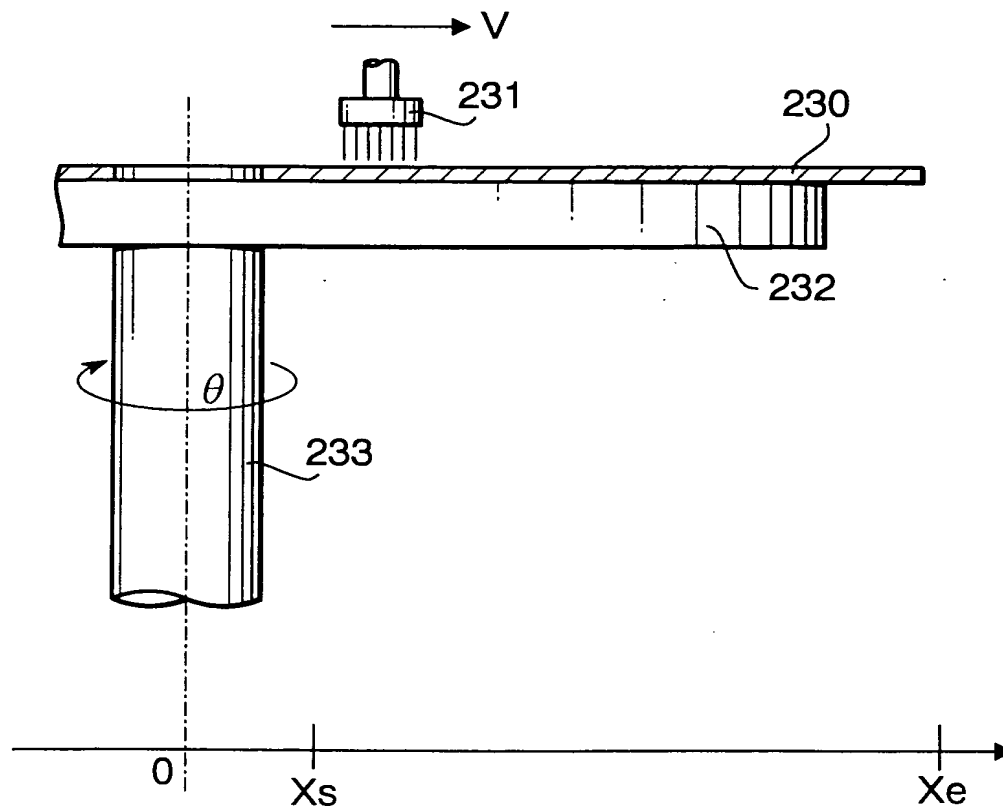


FIG.29  
(PRIOR ART)

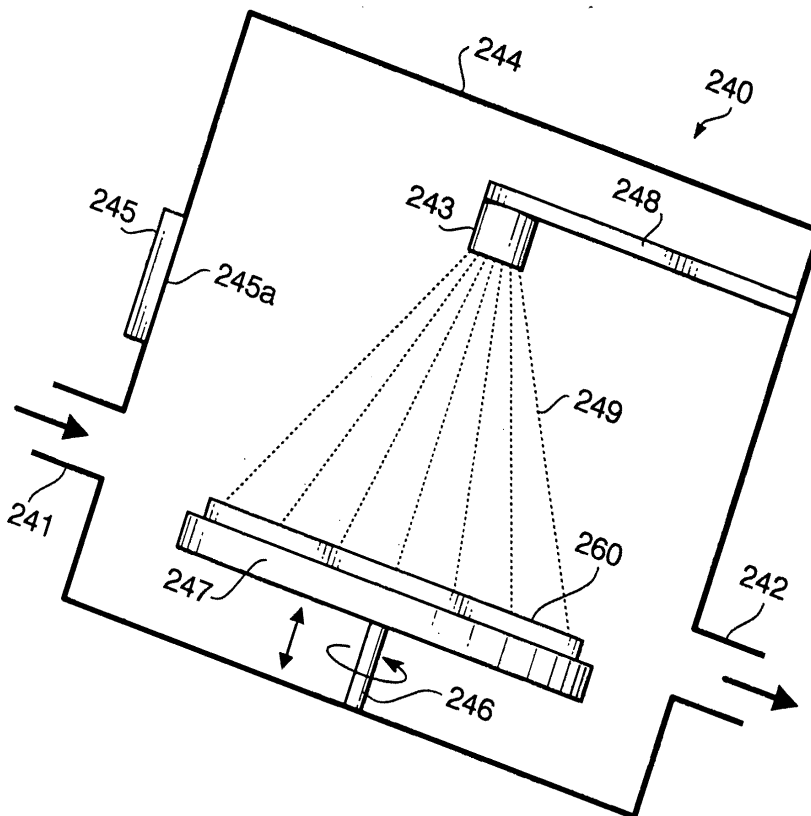


FIG.30  
(PRIOR ART)

